UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,324	06/15/2001	Masahito Tomizawa	10746/27	8427

26646 7590 01/20/2006

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
PEZZLO, JOHN	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,324	TOMIZAWA ET AL.	
	Examiner	Art Unit	
	John Pezzlo	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 18* is/are allowed.

6)☒ Claim(s) *1-5 and 10-14* is/are rejected.

7)☒ Claim(s) *6-8 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

I. Claims 1, 4, 5, 10, 11, 12, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Utsumi (US 4,644,536).

1. Regarding claims 1 and 10 – Utsumi discloses a control pulses generating circuit, (refer to callouts 3, 4, 5, 2, and 1 in Figure 2, and callouts 13, 14, and 15 in Figure 4, and callouts 28 and 29 in Figure 6) which generates control pulses (f Hz clock and the inverse f Hz clock pulses) each of which corresponds to one of said channels, wherein phases of said control pulses are different for each channel, refer to Figure 4 callout 16 and figure 6 callout 31 and column 3 lines 25 to 55, Utsumi discloses the multiplexer which two phases of a clock signal, f Hz, one phase is the inverse of the other phase, refer to the inverter shown in the clock line.

Utsumi discloses channel-frame generating circuits, (refer to callout 4 in Figure 2) connected to said control pulses generating circuit, each of which receives said low-speed frame signal and outputs said low-speed frame signal in synchronization with said control pulse, in the background of the invention, Utsumi discloses a 1/9 Frequency Divider, callout 4 in Figure 2,

which generates a channel-frame generating circuit which generates a low-speed frame signal, refer to Figure 1, F, used in A, B, and C signals and column 1 lines 18 to 65.

Utsumi discloses a multiplexing circuit, connected to said channel-frame generating circuits, which multiplexes said low-speed frame signals into said high-speed serial signal and outputs said high-speed serial signal, refer to callout 8 in Figure 8 and column 1 lines 18 to 65.

2. Regarding claims 4 and 13 – Utsumi discloses synchronization pattern inserting circuits each of which inserts a frame synchronization pattern into said low-speed frame signal, refer to Figures 1 and 2 and column 1 lines 5 to 68 and column 2 lines 1 to 8.

3. Regarding claims 5 and 14 – Utsumi discloses wherein time duration on which said control pulses are generated for every channel is smaller than time duration of channel-frame format, refer to Figure 1 and column 1 lines 5 to 40.

4. Regarding claim 11 – Utsumi discloses demultiplexing said high-speed serial signal into said low-speed frame signals, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses generating, for each of said low-speed frame signals, a frame pulse corresponding to said low-speed frame signal, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses switching the demultiplexer (callout 22 in Figure 5) each of said low-speed frame signals to an appropriate port of said channel according to signals generated from

said frame pulses, the port is inherent, since the demultiplexer outputs two low-speed signals, callouts 26 and 27 in Figure 5, which are assumed to be routed to the destinations through an appropriate port.

5. Regarding claim 12 - Utsumi discloses a control pulses generating circuit, (refer to callouts 3, 4, 5, 2, and 1 in Figure 2, and callouts 13, 14, and 15 in Figure 4, and callouts 28 and 29 in Figure 6) which generates control pulses (f Hz clock and the inverse f Hz clock pulses) each of which corresponds to one of said channels, wherein phases of said control pulses are different for each channel, refer to Figure 4 callout 16 and figure 6 callout 31 and column 3 lines 25 to 55, Utsumi discloses the multiplexer which two phases of a clock signal, f Hz, one phase is the inverse of the other phase, refer to the inverter shown in the clock line.

Utsumi discloses channel-frame generating circuits, (refer to callout 4 in Figure 2) connected to said control pulses generating circuit, each of which receives said low-speed frame signal and outputs said low-speed frame signal in synchronization with said control pulse, in the background of the invention, Utsumi discloses a 1/9 Frequency Divider, callout 4 in Figure 2, which generates a channel-frame generating circuit which generates a low-speed frame signal, refer to Figure 1, F, used in A, B, and C signals and column 1 lines 18 to 65.
Utsumi discloses a multiplexing circuit, connected to said channel-frame generating circuits, which multiplexes said low-speed frame signals into said high-speed serial signal and outputs said high-speed serial signal, refer to callout 8 in Figure 8 and column 1 lines 18 to 65.

Utsumi discloses demultiplexing said high-speed serial signal into said low-speed frame signals, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses generating, for each of said low-speed frame signals, a frame pulse corresponding to said low-speed frame signal, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses switching the demultiplexer (callout 22 in Figure 5) each of said low-speed frame signals to an appropriate port of said channel according to signals generated from said frame pulses, the port is inherent, since the demultiplexer outputs two low-speed signals, callouts 26 and 27 in Figure 5, which are assumed to be routed to the destinations through an appropriate port.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

II. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Utsumi (same as above) in view of Fujimura et al. (US 4,744,082).

1. Regarding claim 2 – Utsumi discloses a demultiplexer which demultiplexes said serial signal into said low-speed frame high-speed signals, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses channel-frame synchronization circuits, the inverse converter, the frame synchronizer, and the frequency divider, shown in Figure 5, connected to said demultiplexer, each of which receives said low-speed frame signal, the 2f Hz clock, generates a frame pulse corresponding to said low-speed frame signal, and outputs said low-speed frame signal, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses a switching circuit, the demultiplexer (callout 22 in Figure 5) connected to said channel-frame synchronization circuits, which receives said low-speed frame signals and sends each of said low-speed frame signals to an appropriate port of said channel, the port is inherent, since the demultiplexer outputs two low-speed signals, callouts 26 and 27 in Figure 5, which are assumed to be routed to the destinations through an appropriate port.

Utsumi does not expressly disclose a switch controller circuit, which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits.

Fujimura discloses a switch controller circuit which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits, refer to Figure 5, callout 220, and Figure 6, and column 6 lines 38 to 68 and columns 7 and 8.

At the time of the invention, it would have been obvious to an ordinary person of skill in the art to combine Fujimura with Utsumi to provide a switch controller circuit which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits. The suggestion for doing so can be found in Utsumi, (background of the invention) which states that the overall circuit arrangement becomes complicated. Therefore, having a switching controller will help to manage the overall operation of the switching circuits.

The motivation and benefit for doing so would be more efficient operation, which is easy to monitor and control.

2. Regarding claim 3 – Utsumi discloses a control pulses generating circuit, (refer to callouts 3, 4, 5, 2, and 1 in Figure 2, and callouts 13, 14, and 15 in Figure 4, and callouts 28 and 29 in Figure 6) which generates control pulses (f Hz clock and the inverse f Hz clock pulses) each of which corresponds to one of said send channels, wherein phases of said control pulses are different for each send channel, refer to Figure 4 callout 16 and figure 6 callout 31 and column 3 lines 25 to 55, Utsumi discloses the multiplexer which two phases of a clock signal, f Hz, one phase is the inverse of the other phase, refer to the inverter shown in the clock line.

Utsumi discloses channel-frame generating circuits, (refer to callout 4 in Figure 2) connected to said control pulses generating circuit, each of which receives said send low-speed frame signal, and outputs said send low-speed frame signal in synchronization with said control pulse, in the background of the invention, Utsumi discloses a 1/9 Frequency Divider, callout 4 in Figure 2, which generates a channel-frame generating circuit which generates a low-speed frame signal, refer to Figure 1, F, used in A, B, and C signals and column 1 lines 18 to 65.

Utsumi discloses a multiplexing circuit, connected to said channel-frame generating circuits, which multiplexes said send low-speed frame signals into said send high-speed serial signal and outputs said send high- speed serial signal, refer to callout 8 in Figure 8 and column 1 lines 18 to 65.

Utsumi discloses a demultiplexer which demultiplexes said receive high-speed serial signal into said receive low-speed frame signals, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses channel-frame synchronization circuits, the inverse converter, the frame synchronizer, and the frequency divider, shown in Figure 5, connected to said demultiplexer, each of which receives said receive low-speed frame signal, the 2f Hz clock, generates a frame pulse corresponding to said receive low-speed frame signal, and outputs said receive low-speed frame signal, refer to Figure 5 and column 3 lines 55 to 68 and column 4 lines 1 to 5.

Utsumi discloses a switching circuit, (callout 22 in Figure 5) connected to said channel-frame synchronization circuits, which receives said receive low-speed frame signals and sends each of said receive low-speed frame signals to an appropriate port of said receive channel, the port is inherent, since the demultiplexer outputs two low-speed signals, callouts 26 and 27 in Figure 5, which are assumed to be routed to the destinations through an appropriate port.

Utsumi does not expressly disclose a switch controller circuit, which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits.

Fujimura discloses a switch controller circuit which controls said switching circuit according to said frame pulses output from said channel-frame synchronization circuits, refer to Figure 5, callout 220, and Figure 6, and column 6 lines 38 to 68 and columns 7 and 8.

At the time of the invention, it would have been obvious to an ordinary person of skill in the art to combine Fujimura with Utsumi to provide a switch controller circuit which controls said switching circuit according to said frame pulses output from said channel-frame

synchronization circuits. The suggestion for doing so can be found in Utsumi, (background of the invention) which states that the overall circuit arrangement becomes complicated. Therefore, having a switching controller will help to manage the overall operation of the switching circuits. The motivation and benefit for doing so would be more efficient operation, which is easy to monitor and control.

Allowable Subject Matter

Claims 9 and 18 are allowable over the prior art of record.

Claims 6, 7, 8, 15, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 27 December 2005 have been fully considered but they are not persuasive. On page 4 of the response applicants argue that the reference (Utsumi) does not identically describe the features of claim 1. The examiner respectfully disagrees. Utsumi discloses the use of clock pulses, which are used as control pulses as pointed out by the examiner. All the elements of claim 1 are explicitly disclosed by Utsumi as pointed out in the rejection. The examiner has referenced callouts 3, 4, 5, 2, and 1 in Figure 2 and callouts 13, 14,

and 15 in Figure 4, and callouts 28 and 29 in Figure 6 which are control pulses, f Hz clock and the inverse f Hz clock pulses, wherein the phases of said control pulses are different for each channel as shown in the Figures. The examiner has not invoke inherency and the examiner has shown how claim 1 reads on the reference.

Claim 2 is rejected using two references Utsumi in view of Fujimura (a 103 rejection), the examiner has made a *prima facie* case, which is proper and meets the guidelines set forth in *Graham vs. Deere*. The examiner has show there is a suggestion and motivation to utilize a switch controller circuit of Fujimura, which Utsumi is lacking.

All the rejections are proper therefore, this action is made final.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Pezzlo whose telephone number is (571) 272-3090. The examiner can normally be reached on Monday to Friday from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C.

or faxed to:

(571) 273-8300

For informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand delivered responses should be brought to:

Jefferson Building

2A15

500 Dulany Street

Alexandria, VA, 22313.

John Pezzlo

19 January 2006

JOHN PEZZLO
PRIMARY EXAMINER